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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/741,857	12/22/2000	Richard P. Modelski	120-100	8573

34845 7590 03/19/2008
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EXAMINER
TRUONG, LAN DAI T

ART UNIT	PAPER NUMBER
2152	

NOTIFICATION DATE	DELIVERY MODE
03/19/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	09/741,857	MODELSKI ET AL.	
	Examiner	Art Unit	
	LAN-DAI Thi TRUONG	2152	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *none* is/are allowed.

6)☒ Claim(s) *1-3 and 5-18* is/are rejected.

7)☐ Claim(s) *none* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/29/2007 has been entered.

2. This action is response to communications: application, filed on 12/22/2000; amendment filed 11/29/2007. Claims 1-3, 5-18 are pending; claims 1-3, 5, 17 are amended; claim 4 is canceled

3. The applicant's arguments filed on 11/29/2007 have fully considered but they are moot in view with new ground for rejections

Claim rejections-35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matters (e.g. "multi-IP packet thread"; "responsive to an activity status of the first multi-IP packet thread, forwarding the first multi-IP packet thread to next stage") those were not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Nowhere in the specification disclosed the use of multi-IP packet threads. The specification, at most, discloses the use of "IP packet", but is completely silent in regards to "multi-IP packet threads". Without the disclosure of multi-IP packet threads, how would one of ordinary skill in the art determine to forward the multi-IP packet thread to next stage? Furthermore, how is the forwarding in responsive to an active status of the first multi-IP packet thread is processed if nothing in the specification disclose about the use of multi-IP packet thread?

5. Claim 5 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matters (e.g. "multi-IP packet thread"; "processing pipeline selectively forwards the multi-IP packet threads through the processing pipelines in responsive to the activity status of the multi-IP packet thread") those were not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. As same as section 4, nowhere in the specification disclosed the use of multi-IP packet threads. The specification, at most, discloses the use of "IP packet", but is completely silent in regards to "multi-IP packet threads". Without the disclosure of multi-IP packet threads, how would one of ordinary skill in the art determine to operate the multi-IP packet threads in a

processing pipeline including a plurality of stages. Furthermore, how processing pipeline selectively forwards the multi-IP packet threads through the processing pipelines in responsive to the activity status of the multi-IP packet thread if nothing in the specification disclose about the use of multi-IP packet thread?

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1 and 5 recite the limitation "multi-IP packet thread" (in claim 1, lines 3, 5-10; claim 5, lines 1-2, 4-11). There is insufficient antecedent basis for this limitation in the specification.

Claim rejections-35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or descried as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3 are rejected under 35 U.S.C 103(a) as being un-patentable over Davis et al. (U.S. 5,357,617) in view of Kelsey et al. (U.S. 2002/0002667) and further in view of Kessner (U.S. 6,754,701)

Regarding claim 1:

Davis discloses the invention substantially as claimed, including a method, apparatus and system, which can be implemented in a computer hardware or software code for processing a plurality of independent multi-packet threads comprising:

processing a first multi thread in a first stage of a processing pipeline; forwarding a first thread to a next stage of the processing pipeline while forwarding a second packet thread to the first stage of the processing pipeline such that the first and the second threads can be processed simultaneously in the processing pipeline; and wherein the independence of the multi packet threads eliminates IP packet processing delays: (Davis discloses a pipeline processor for simultaneously processing of a plurality of threads. The pipelined processor includes number of different stages (e.g. fetching, decoding and executing). The Davis's system processes subsequent steps of: fetching instruction of a first thread from numbers of threads, decoding the fetched instruction of the first thread while fetching instruction of a second thread from number of the threads…and so on. Davis also mentions his invention pipelined processor can be used for eliminating time delay purpose: column 3, lines 15-36; column 2, lines 1-9)

However, Davis does not explicitly disclose assigning a thread identifier (TID) to each of independent multi threads and maintaining an activity status for each thread; responsive to an activity status of the first multi-IP packet thread, forwarding the first multi-IP packet thread to next stage

In analogous art, Kelsey discloses method of using tables to store activity/ or available thread identifiers those used by a thread selector to forward the selected active thread into the

processing pipeline, see (figure 10, item 8; figure 12; figure 11; [0073], lines 9-31; [0074]-[0075]; [0081])

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Kelsey's ideas of selecting active thread from available thread identifier table for forwarding the selected active thread into a process pipeline into Davis's system in order to improve more advantages into Davis's system (e.g. reducing memory utilization, faster response times and reducing input and output time delay), see (Kelsey: [0023])

However, Davis-Kelsey does not explicitly disclose multi-IP thread

In analogous art, Kessner discloses a processing pipeline including multiple stages; therefrom multi-IP thread is forwarded through the multiple stages in order to finish its task, see (figure 3, item 308; figure 4; column 5, lines 62-65; column 6, lines 1-29)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Kessner's ideas of implying multiple stages process pipeline technique into IP threads into Davis-Kelsey's system in order to increase efficiencies into web services (e.g. reducing resource utilizations), see (Kessner: column 1, lines 8-12)

Regarding claim 3:

In addition to rejection in claim 1, Davis-Kelsey-Kessner further discloses the activity status indicates one of active, inactive or waiting: (Kelsey: [0073]-[0075])

Claim 2 is rejected under 35 U.S.C 103(a) as being un-patentable over Davis-Kelsey-Kessner in view of Epps et al. (U.S. 6,813,243)

Regarding claim 2:

Davis-Kelsey-Kessner discloses the invention substantially as disclosed in claim 1, but does not explicitly teach steps of transferring the multi-IP packet thread from an input buffer to a packet task manager; dispatching the multi-IP packet thread from the packet task manager to an analysis machine; classifying the multi-IP packet thread in the analysis machine; and modifying and forwarding the multi-IP packet thread in a packet manipulator

In analogous art, Epps teaches methods for transferring data from an input buffer (Fig 2, item 215) to a packet task manager (Fig 2, items 130, 285, 280; figure 4; column 7, lines 10-44; Column 5, lines 50-55); dispatching the data from the packet task manager to an analysis machine (figure 4; column 7, lines 44-67); classifying the data in the analysis machine (Column 6, lines 33-37); and modifying and forwarding the data in a packet manipulator (figure 4; column 7, lines 44-67); a packet manipulator (Epps, Figure 4, items 450, 460) operationally connected to said analysis machine (Epps, Figure 4)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Epps's those ideas into Davis-Kelsey-Kessner's system in order to increase efficiencies for data transmission network (e.g. maximum transmission speed), see (Epps: column 3, lines 5-7, lines 40-45)

Claims 5, 17 are rejected under 35 U.S.C 103(a) as being un-patentable over Kelsey et al. (U.S. 2002/0002667) in view of Kessner (U.S. 6,754,701) and further in view of Davis et al. (U.S. 5,357,617)

Regarding claim 5:

Kelsey discloses the invention substantially as claimed, including an apparatus, which can be implemented in a computer hardware or software code for enabling multithreading in embedded processor, comprising:

a processing pipeline including a plurality of stages coupled to receive and process the plurality of independent multi threads such that during a processing period, each of the plurality of stages of the processing pipeline is operating on a different one of the multi threads from the plurality of multi threads: (in Keysley's system, there are different stages exist within a processing pipeline. Keysley's system permits multiple threads to exist in the pipeline concurrently and at different stages: [0049], lines 7-10; [0047], lines 1-3; [0017])

storage for storing data associated with each of the multi threads, the data including a thread identifier (TID) and an activity status for each of the multi threads, wherein processing pipeline selectively forward the multi threads through the processing pipeline in response to the activity status of the multi thread: (in Kelsey's system, activity or available thread identifiers are stored in tables those used by thread selector to select and forward the selected active thread into the processing pipeline: figure 10, item 8; figure 12; figure 11; [0073], lines 9-31; [0074]-[0075]; [0081])

However, Kelsey does not explicitly discloses multi-IP thread

In analogous art, Kessner discloses a processing pipeline processing pipeline including multiple stages; therefrom, multi-IP thread processes through the multiple stage in order to finish its task, see (figure 3, item 308; figure 4; column 5, lines 62-65; column 6, lines 1-29)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Kessner's ideas of implying multiple stages processing pipeline

into IP threads into Keysley's system in order to increase efficiencies into web services (e.g. reducing resource utilizations), see (column 1, lines 8-12)

However, Kelsey- Kessner does not clearly point out for eliminating pipelines processing delays purpose

In analogous art, Davis discloses a pipeline processor including number of different stages (e.g. fetching, decoding and executing) for simultaneously process numbers of threads. Davis mentions his invention pipelined processor can be used for eliminating time delay, see (column 3, lines 15-36; column 2, lines 1-9)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Davis's ideas of using a pipeline processor for simultaneously processing of a plurality of threads into Kelsey- Kessner's system in order to reduce processing time delay, see (Davis: column 2, lines 1-10)

Regarding claim 17:

In addition to rejection in claim 5, Kelsey-Kessner-Davis further discloses the activity status indicates one of active, inactive or waiting: (Kelsey: [0073]-[0075])

Claims 6-16, 18 are rejected under 35 U.S.C 103(a) as being un-patentable over Kelsey-Kessner-Davis in view of Epps et al. (U.S. 6,813,243) and further in view of Fleck et al. (U.S. 6,292,845)

Regarding claim 6:

Davis-Kelsey-Kessner discloses the invention substantially as disclosed in claim 5, but does not explicitly teach a packet manager operatively connected to said analysis machine; and packet manipulator operationally connected to said analysis machine

In analogous art, Epps discloses a packet task manager (Epps, Figure 2, item 130, Column 5, lines 50-55) operationally connected to said analysis machine (Epps, Figure 2; Column 6, lines 33-37); a packet manipulator (Epps, Figure 4, items 450, 460) operationally connected to said analysis machine (Epps, figure 3; fig 4, column 15, lines 32-67; column 7, lines 12-67; column 8, lines 1-67; column 9, lines 1-67; column 10, lines 1-67).

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Epps's those ideas into Davis-Kelsey-Kessner's system in order to increase efficiencies for data transmission network (e.g. maximum transmission speed), see (Epps: column 3, lines 5-7, lines 40-45)

However, Davis-Kelsey-Kessner- Epps does not explicitly disclose a machine having multiple pipelines; wherein one pipeline is dedicated to directly manipulating individual data bits of a bit field;

In analogous art, Fleck's system including multiple pipelines: (column 3, lines 61-67; column 4, lines 1-67; column 5, lines 59-62; column 6, lines 7-34)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Fleck's ideas of including multiple pipelines into Davis-Kelsey-Kessner- Epps's system in order to increase efficiencies for data transmission system, see (Fleck: column 3, lines 61-67)

Regarding claim 7:

In addition to rejection in claim 6, Davis-Kelsey-Kessner- Epps- Fleck further discloses the activity status indicates one of active, inactive or waiting: (Kelsey: figure 8)

Regarding claim 8:

In addition to rejection in claim 6, Davis-Kelsey-Kessner- Epps- Fleck further discloses 32 threads, although Davis-Kelsey-Kessner- Epps- Fleck does not specifically disclose analysis machine has 32 threads, such limitations are merely a matter of design choice and would have been obvious in system of Davis-Kelsey-Kessner- Epps- Fleck

Regarding claim 9:

In addition to rejection in claim 6, Davis-Kelsey-Kessner- Epps- Fleck further discloses a packet task manager (Epps, Figure 2, item 130; Column 5, lines 50-55) operationally connected to said analysis machine (Epps, Figure 2; Column 6, lines 33-37); a packet manipulator (Epps, Figure 4, item 450, 460) operationally connected to said analysis machine (Epps, Figure 4); a global access bus including a master request bus (Epps, Figure 4, item 496) and a slave request bus (Epps, Figure 4, item 497) separated from each other and pipelined (Epps, Figure 4, items 410-460)

Regarding claim 10:

In addition to rejection in claim 6, Davis-Kelsey-Kessner- Epps- Fleck further discloses an external memory engine (Figure 4, item 215) operationally connected to said analysis machine (Epps, Figure 4, item 420; Column 6, lines 30-35) wherein the analysis machine classifies packet data; a hash engine (Epps, Figure. 4, item 430; Column 24, lines 24-28) operationally connected to said analysis machine (Epps, Column 24, lines 24-48)

Regarding claim 18:

In addition to rejection in claim 9, Davis-Kelsey-Kessner- Epps- Fleck further discloses a bi-directional access port operationally connected to said analysis machine (Epps, Column 25, lines 1-7, wherein the input/output port are PPP/HDLC); an input buffer (Epps, Figure 2, item 215) operationally connected to said analysis machine (input buffer operationally connected to Prep Stage: Figure 4, item 420 / analysis machine through the pipeline); and an output buffer (Epps, Fig 2, item 1430) operationally connected to said analysis machine (transmit FIFO operationally connected to Prep Stage Figure 4, item 420 through the switch fabric)

Regarding claims 11:

In addition to rejection in claim 9, Davis-Kelsey-Kessner- Epps- Fleck further discloses packet input global access bus program code, stored in a computer readable memory and operable when executed to control a flow of data packet information from a flexible input data buffer to the analysis machine (Epps: wherein the instructions are the software code: Column 4 44, lines 60-67; Column 45, lines 1-15)

Regarding claims 12-16:

Those claims are rejected under rationale of claim 11

Conclusions

The prior arts made of records and not relied upon are considered pertinent to applicant's disclosure. The following patents and publications are cited to further show the state of the art with respect to "Multi-thread packet processor": 6938147; 6609193; 6542991; 6470443; 6463522; 634134; 6240509; 6073159; 5996068; 6212542; 7110773 ; 20030158900; 0020188714; 20020099842;

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan-Dai Thi Truong whose telephone number is 571-272-7959. The examiner can normally be reached on Monday- Friday from 8:30am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bunjob A. Jaroenchonwanit can be reached on 571-272-3913. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

02/12/2008

/Kenny S Lin/
Primary Examiner, Art Unit 2152